



A Thirteen Level Inverter Design Based on Hybrid MLI Topology for Minimum THD

S.LakshmiPriya¹, R.K.Raghav², Dr.M.Muruganandam³

PG Student, Dept. of EEE, Muthayammal Engineering College, Rasipuram, Tamilnadu, India ¹

Assistant Professor, Dept. of EEE, Muthayammal Engineering College, Rasipuram, Tamilnadu, India ²

Professor, Dept. of EEE, Muthayammal Engineering College, Rasipuram, Tamilnadu, India ³

ABSTRACT: To minimize the power demand and scarcity we have to improve the power extracting methods. Multilevel inverter is used to extract power from solar cells, fuel cells and batteries. It synthesizes the desired ac output waveform from several dc sources. This paper presents a three phase hybrid multilevel inverter topology that uses thirteen level transistor clamped H-Bridge with minimum total harmonic distortion. To achieve a better voltage utilisation and harmonics reduction, Multicarrier Phase Shift Pulse Width Modulation control technology is used. The analysis of output voltage harmonics and the total power losses converging the switching power losses are carried out and compared with the cascaded neutral point clamped and conventional H-Bridge inverters. A new method to balance the system voltage in each source is developed and tested. For the verifications it is tested on three phase application systems. From the results, the proposed inverter provides higher output quality with relatively less harmonics losses and THD as compared to the other conventional inverters.

KEYWORDS: Hybrid H-bridge, multicarrier phase-shifted pulse-width modulation, multilevel inverter, transistor-clamped converter.

I. INTRODUCTION

Multilevel converters are mainly used to synthesis a required single or three-phase voltage waveform. The required multi-staircase output voltage is obtained by combining several balanced dc voltage sources. The most commonly used independent sources are Solar cells, fuel cells, batteries and ultra-capacitors [1]. One important application of multilevel converters is mainly concentrated on medium and high-power conversion systems. Now a day, there exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC) or diode clamped inverter, cascaded H-bridge (CHB), and flying capacitors (FCs) [2]. Among these three topologies, cascaded multilevel inverter reaches the higher output voltage and power levels and the higher reliability due to its modular topology [3]. Diode-clamped multilevel converters are utilized in conventional high-power ac motor drive applications like conveyors, pumps, fans and mills. NPC also plays a vital role in oil, gas, metals, power, mining, and water, marine and chemical industries. In regenerative system also the NPC multilevel inverter is used in back to back configuration [4]. Flying capacitor multilevel converters have been used in high bandwidth high-switching frequency applications such as medium-voltage traction drives. Finally, hybrid cascaded H-bridge multilevel converters have been applied where high power and power quality are essential, for example, static synchronous compensators active filter, reactive power compensation applications, uninterruptible power supplies, photovoltaic power conversion and magnetic resonance imaging. One of the growing applications for multilevel motor drives is electric and hybrid power transient. For increasing voltage levels, the number of switches also will increase in number. Hence this leads to voltage stress and switching loss. For minimizing these losses we have to add filters, this process makes the circuit will become complex. By using the proposed topology, number of switches will reduce significantly and increase the efficiency of the system [5]. In high power applications, the harmonic content of the output waveforms has to be reduced as much as possible in order to avoid distortion in the grid and it will reach the maximum energy efficiency [6].

The first multilevel inverter was introduced in three level converters. A multilevel converter is a power electronic system using several levels of dc voltages as inputs to synthesize a desired output voltage; the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The

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primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, lower switching losses and better electromagnetic computability [7]. The transistor clamped converter topology has received increased attention as it provides a simpler approach to increase output levels by taking different voltage levels from the series stacked capacitors [8 & 9]. In this paper, the proposed new configuration uses a thirteen-level transistor-clamped H-bridge (TCHB) that can produce a thirteen-level output instead of five-level as with the conventional H-bridge[10-12]. A

similar arrangement using a NPC in each power cell has been presented [13-17]. However, for the efficient output an excessive number of power switches and diodes are required. Cascaded hybrid H-bridge multilevel inverters increases the voltage levels, reduce losses and used for industrial application. The general configuration is shown in the figure 1.1

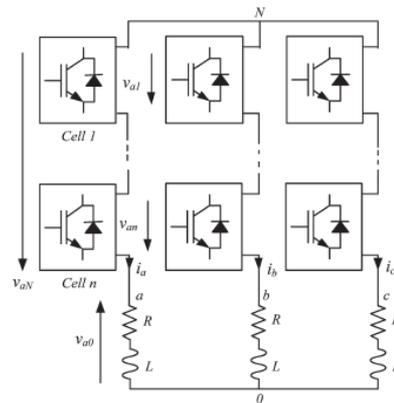


Fig 1.1 General configuration of the proposed three phase cascaded multilevel inverter

II. PROPOSED INVERTER CONFIGURATION

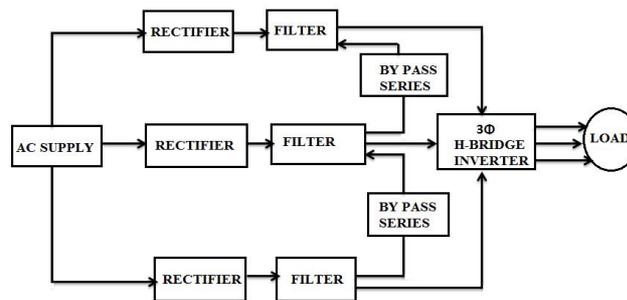


Fig 2.1 Block diagram of proposed inverter

In addition to the better output quality, with more output levels, the possibility of insulation failure is reduced across the motor terminals compared to the conventional CHB with similar configuration. It mainly focus on the constant speed drive applications such as fans, blowers, pumps and compressors, since these comprise 97% of currently installed medium voltage drives. It is found in various industries such as process industries, production plants as well as in oil and gas sectors. The proposed method mainly reduced the components used and concentrates on the better voltage utilization. It also reduces the switch counts, total harmonic distortion and reduces the losses. The figure 2.1 explains as follows, In order to converter the ac source into dc source rectifier is used in between the filter and ac source. The filter is mainly used to reduce the harmonics and other unwanted noise .The bypass series filter is mainly used for isolating purpose of the switches to be turned ON. Based on turning ON and turning off the switches the output voltage level is increased and the cascaded 13-level multilevel inverter is shown in the figure 2.2.

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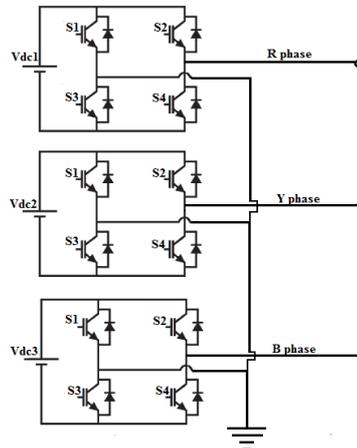


Fig 2.2 Cascaded 13-level multilevel inverter

In general, the maximum levels in the phase and line voltages of the proposed inverter, based on NC (series-connected five levels TCHB) cells, are given by the following equations.

$$n_p = 4N_c + 1 \quad (1)$$

$$n_p = 8N_c + 1 \quad (2)$$

Based on valid switching combinations s_1-s_5 , the cell output voltage can be represented by

$$V_{an} = V_{dc} (S_{5n} - S_{4n}) \left\{ \frac{1}{2} S_{2n} + |S_{2n} - S_{4n}| |S_{2n} - S_{5n}| \right\} \quad (3)$$

III .PWM MODULATION STRATEGY

Pulse-Width Modulation (PWM) or pulse-duration modulation (PDM), is a modulation technique that controls the width (in time) of an electrical pulse, formally the pulse's duration, based on modulator signal information. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors. In addition, PWM is one of the two principal algorithms used in photovoltaic solar battery chargers, the other being MPPT. The modulation index M of the proposed multilevel inverter is defined by

$$M = \frac{v_{ref}}{v_{cr}} \quad (4)$$

Where v_{ref} is the amplitude of the voltage reference and v_{cr} is the amplitude of the carrier signal. Multicarrier phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals.

A.Phase Shift PWM (PSPWM)

The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. In addition to the phase shift modulation, level shift modulations also exist in order to eliminate the harmonics of the output waveform. This scheme does not require any modification in the carrier or modulating signal. It has advantage or superiority over other previous works. But there is a phase shift between any two adjacent carrier waves. For m Voltage levels $(m-1)$ carrier signals are required and they are phase shifted with an angle of $\theta = (360^\circ / (m-1))$. The gate signals are generated with proper comparison of carrier wave and modulating signal and it is shown in figure 3.1.

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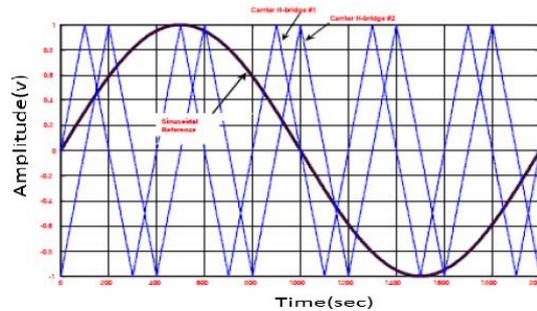


Fig 3.1 Phase shifted carrier PWM

B. Level shifted PWM (LSCPWM)

For carriers signals, the time values of each carrier waves are set to $[0 \ 1/600 \ 1/300]$ while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBT. This technique is divided into 3 types, they are i) In Phase disposition (IPD) ii) Phase opposition disposition (POD) iii) Alternate phase opposition disposition (APOD)

i. In Phase disposition (IPD)

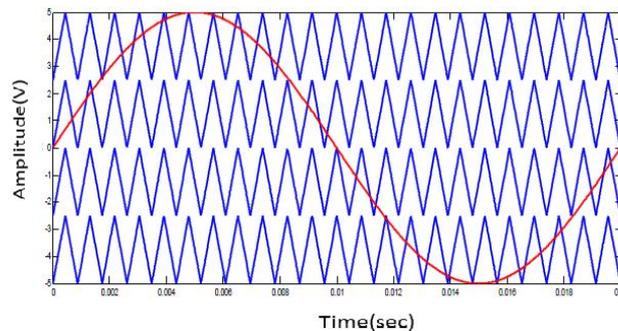


Fig 3.2 Carrier arrangement for PDPWM

In this method all the carriers signals above and below zero reference line are in same phase. If all the carriers are selected with the same phase, then the method is known as Phase Disposition (PD) method. Carrier and reference wave arrangements are as shown in Fig.3.2. It is the most widely used strategy for Modular Multilevel converters and conventional multilevel inverters because it provides load voltage and current with lower harmonic distortion and switching losses.

ii. Phase opposition disposition (POD)

In this method all the carriers have the same frequency and the adjustable amplitude (unequal amplitude and difference with phase sequence). But all the carriers above the zero value reference are in phase among them but in opposition (180 degrees phase shifted) with those below. Carrier and reference wave arrangements are as shown in figure 3.3.

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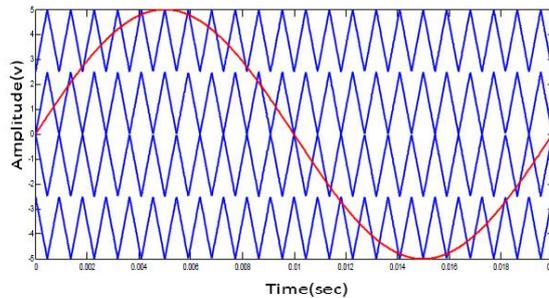


Fig 3.3 Carrier arrangement for PODPWM strategy

iii. Alternate phase opposition disposition (APOD)

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). There is 180 degree phase shift between all the carrier signals.

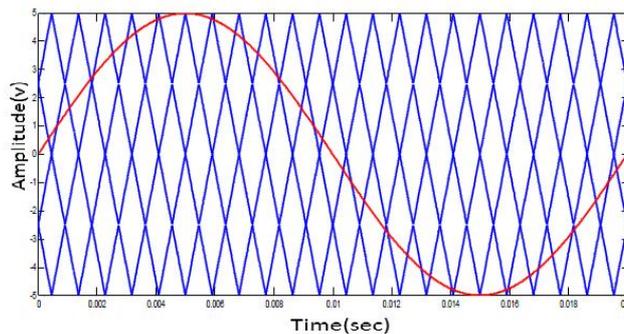


Fig 3.4. Carrier arrangement for APODPWM strategy

The carrier waves and the modulating signals are compared and the output of the comparator defines the output in the positive half cycle the comparator output will have the value high, if the amplitude of the modulating signal is greater than that of the carrier wave and zero otherwise and it is shown in figure 3.4. Similarly for the negative half cycle, if the modulating signal is lower than the carrier wave the output of the comparator is high and zero otherwise.

IV. LINE-VOLTAGE THD

Regarding the switching frequency of multilevel inverters, two categories are classified based on the switching strategies: strategies that work with high switching frequencies, including the classical carrier-based sinusoidal pulsewidth modulation (PWM) strategy, and those that work with low switching frequencies, generally equal to the fundamental component frequency, and generate a staircase waveform. Representatives of this category are the so-called “optimized harmonic stepped waveform”, “selective harmonic mitigation PWM” and “optimal minimization of the total harmonic distortion”. Although this category is not necessarily restricted to the fundamental frequency and higher switching frequencies can be employed in order to improve harmonic conditions, but in this section, fundamental frequency switching is considered. The extension can be made with higher switching frequencies categories. The most efficient method is OMTHD, by which the waveform THD is minimized by determining the switching angles while the desired fundamental component is generated. To achieve this, an optimization algorithm is employed, in which the objective is to minimize harmonics. THD and either the fundamental component is considered as a constraint or its error is added to the objective function. THD is defined as the ratio of all harmonic components rms value to the fundamental component value and is expressed as follows:

$$(THD)_p = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad (5)$$

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The aim is to determine the optimum switching angles that generate an output voltage with the required fundamental component and the possible minimum THD. This is a problem to be solved by an optimization algorithm.

Parameters	Multilevel Inverters			
	five level inverter	Seven level inverter	Eleven level inverter	Thirteen level inverter(proposed method)
Voltage level	166.3	248.7	406.7	420
THD for voltage	29.00%	20.82%	16.31%	7.34%

TABLE 4.1 THD of five, seven, eleven and thirteen level inverters

The above table shows the voltage and the total harmonic distortion for various multilevel inverters.

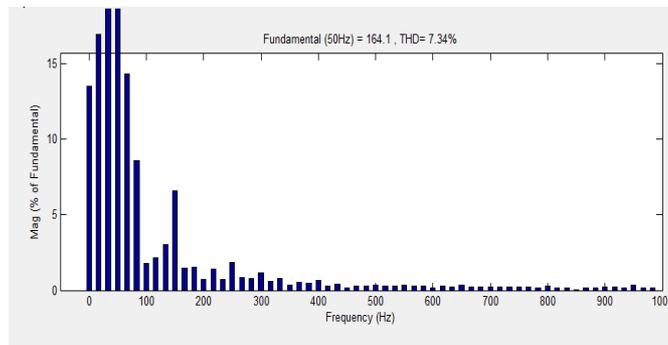


Fig 4.2 THD Calculation for thirteen levels

The figure 4.2 shows the total harmonics distortion (7.34%) for thirteenlevels. It is reduced from 29% to 7.34% for various levels. Along with the total harmonics distortion we are improving the output voltage with balanced dc source from 406V to 420V.

V. ANALYSIS OF SIMULATION RESULTS

The simulation result was analysed in both single and three phases by reducing the number of switches and the switch count with high efficiency and low power losses. In order to analysis the each level of multilevel inverter multicarrier phase shift pulse width modulation is used to reduce the harmonics of the output voltage waveform. In order to produce only the positive cycle waveform we have to activate the transistor clamped switches. For high power application mosfet is used as a switching device. The second order filter is used to reduce the output harmonics and it is shown in the figure 5.1.

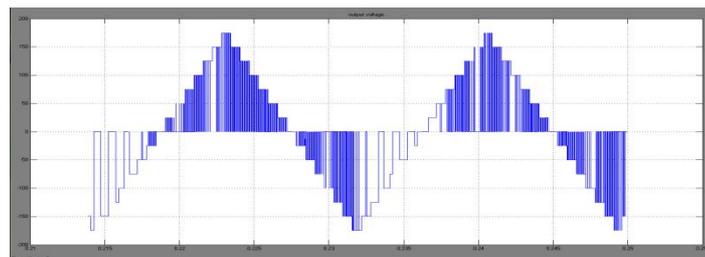


Fig 5.1 Positive and negative cycle's waveforms for single phase

In electronics, counters can be implemented quite easily using register-type circuits such as the flip-flop. The up/down counter is designed by JK flip-flop for producing toggle state. The up/down counters with NOT gate combination used

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to increment and decrement the levels both in positive and negative cycles. The multicarrier phase pulse width modulation is made with the comparison of fundamental and carrier signal. This makes the pulse width modulation in each level of the inverter.

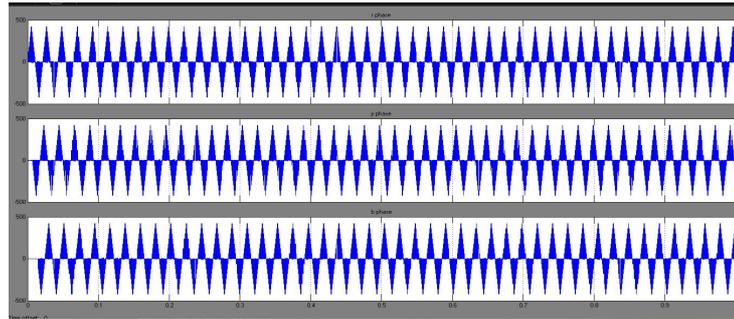


Fig 5.2 Simulated output for R, Y, B phase

Finally, with less number of switches the multilevel output is created for thirteen level with less harmonics and distortion. The harmonics distortion is reduced about 7.34% and it is shown in the figure 5.2.

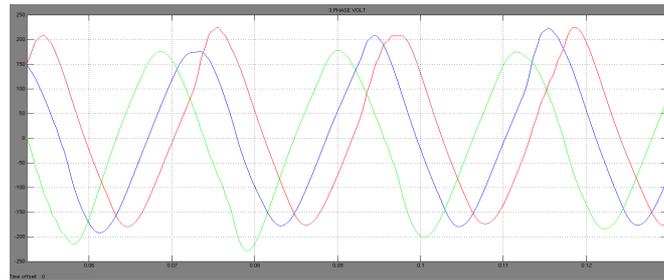


Fig 5.3 Simulated waveform for three phase volt

The voltage is increased up to 420V. Normally the output is in the form sinusoidal waveform and it is shown in the figure 5.3. The distortion of a waveform relative to a pure sine wave can be measured either by using a THD analyser to analyse the output wave into its constituent harmonics and noting the amplitude of each relative to the fundamental; or the notch filter cancelling the fundamental and measuring the total aggregate harmonic distortion plus noise which will be the remaining signal.

VI. CONCLUSION

In this paper, multilevel inverter configuration based on a thirteen-level TCHB inverter with multicarrier phase shifted PWM modulation technology, is analyzed and presented. A new method hybrid cascaded multilevel inverter was developed and tested with balanced DC source for better voltage utilization. The output voltages of the proposed inverter were analysed in various operating conditions. Detailed comparisons between the proposed inverter, NPC, 5L-CHB and 9L-CHB in terms of power quality, power losses and total harmonic distortions also analysed. From the observations, the proposed inverter is found potential not only for medium-voltage drive application but also other applications like high voltage drives demanding higher output quality.

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